

FIGURE 1  
(PRIOR ART)

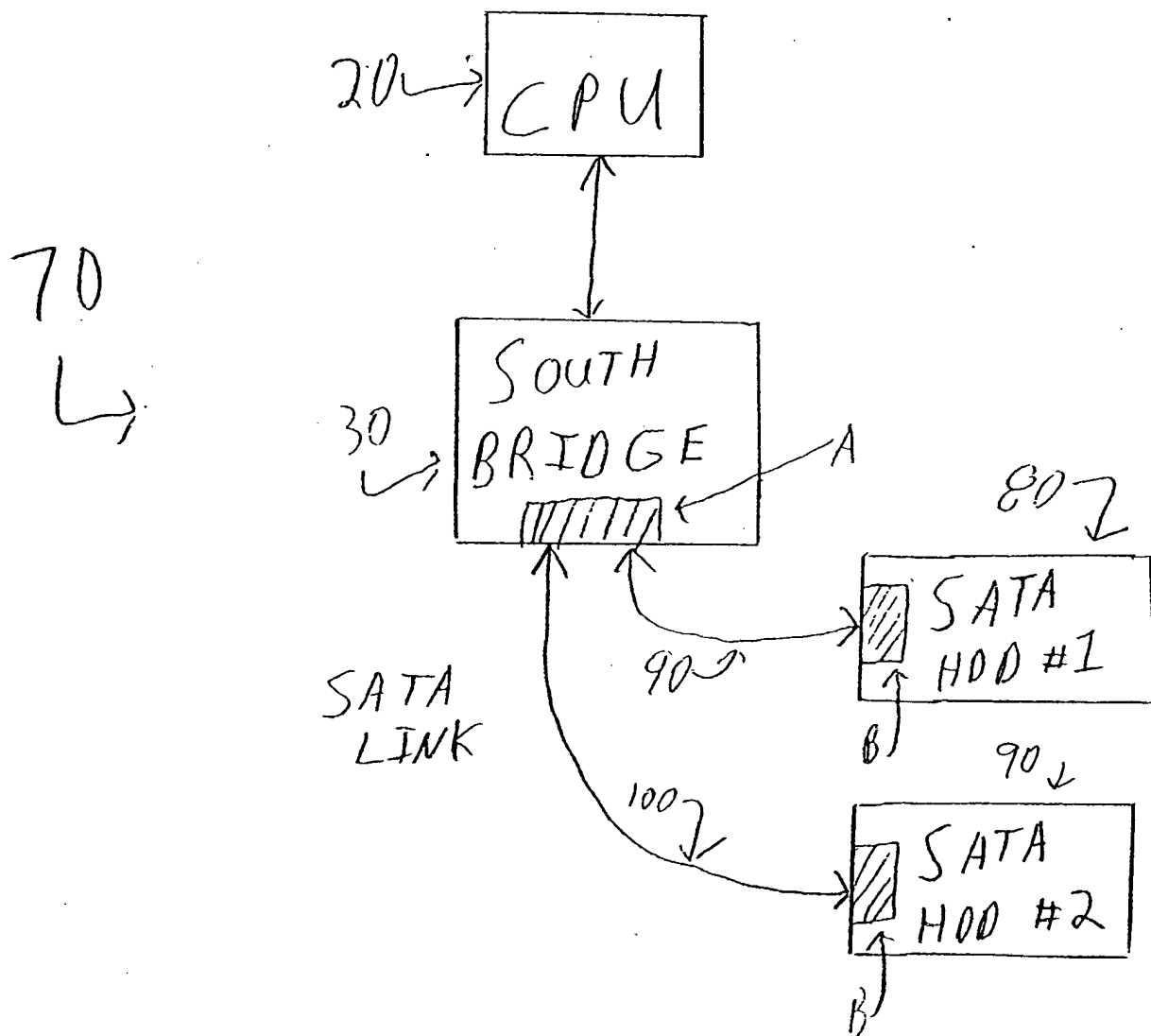
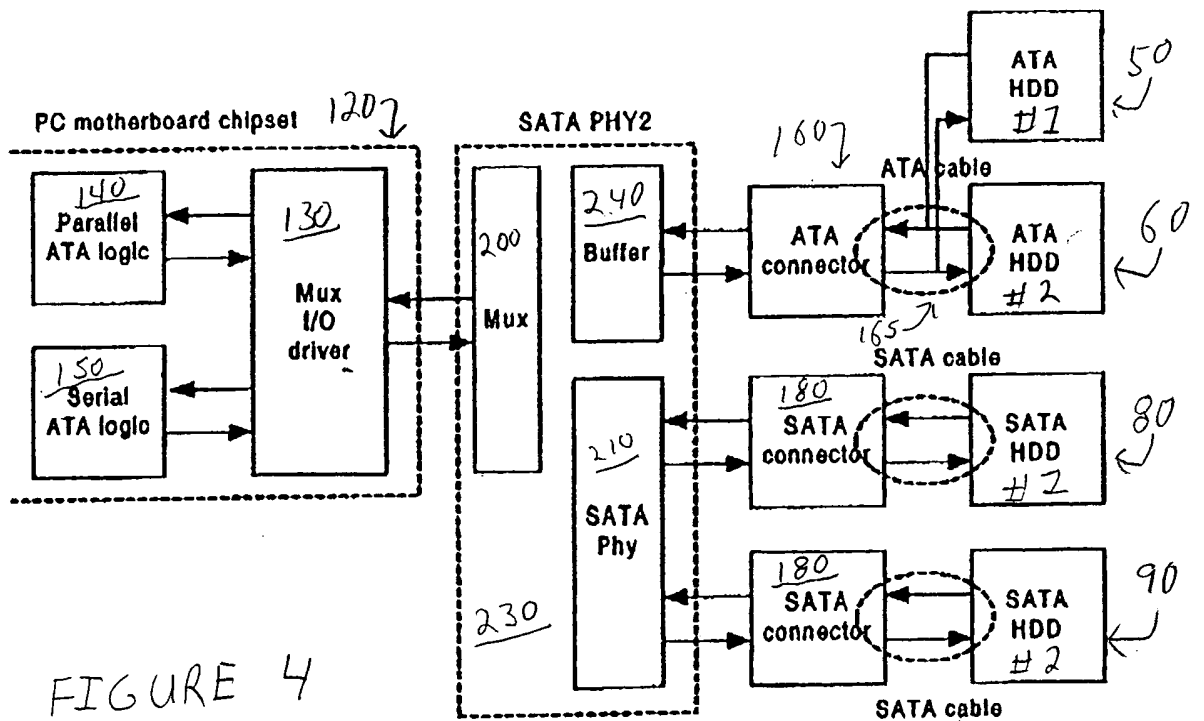
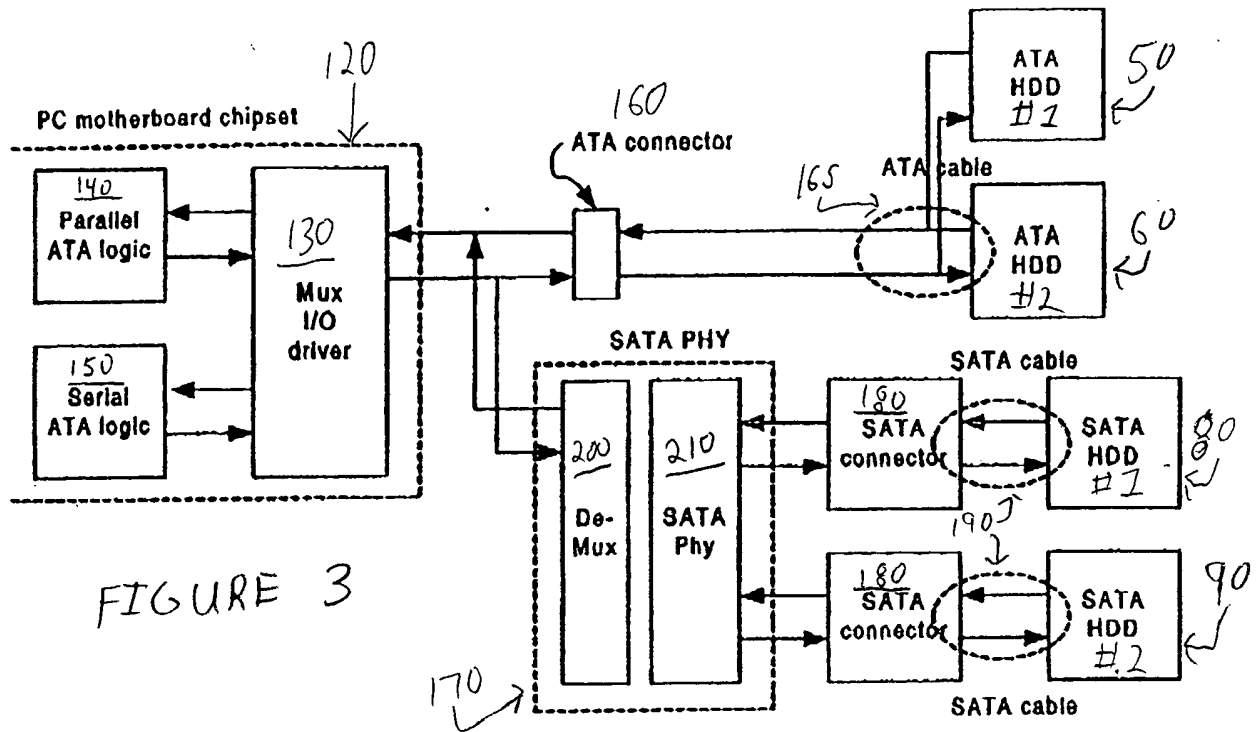


FIGURE 2  
SATA LINKED SYSTEM  
(PRIOR ART)



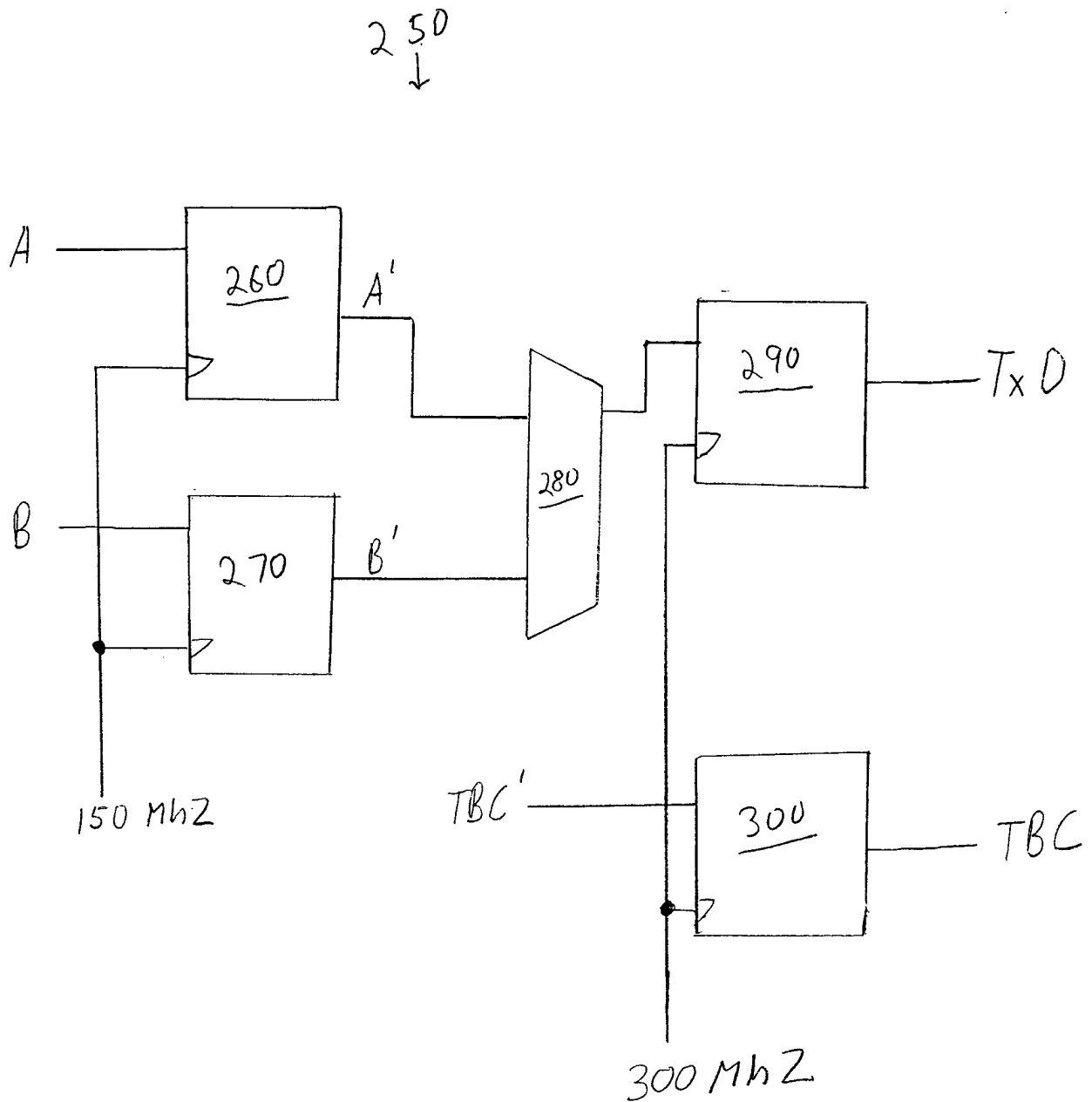
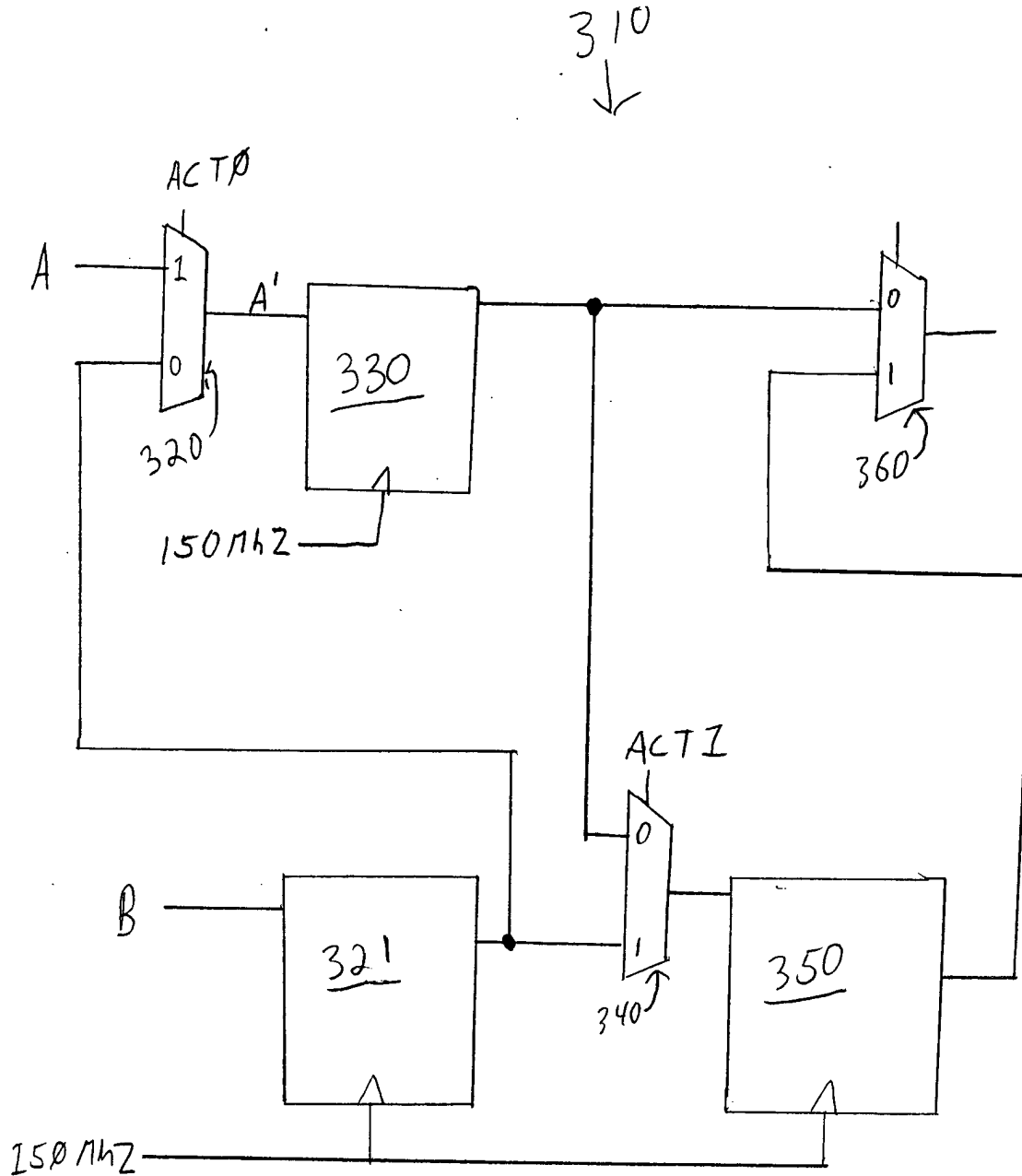


FIGURE 5A



ACT0	ACT1	
1	1	double data rate
0	1	single data rate
1	0	single data rate

FIGURE 5B

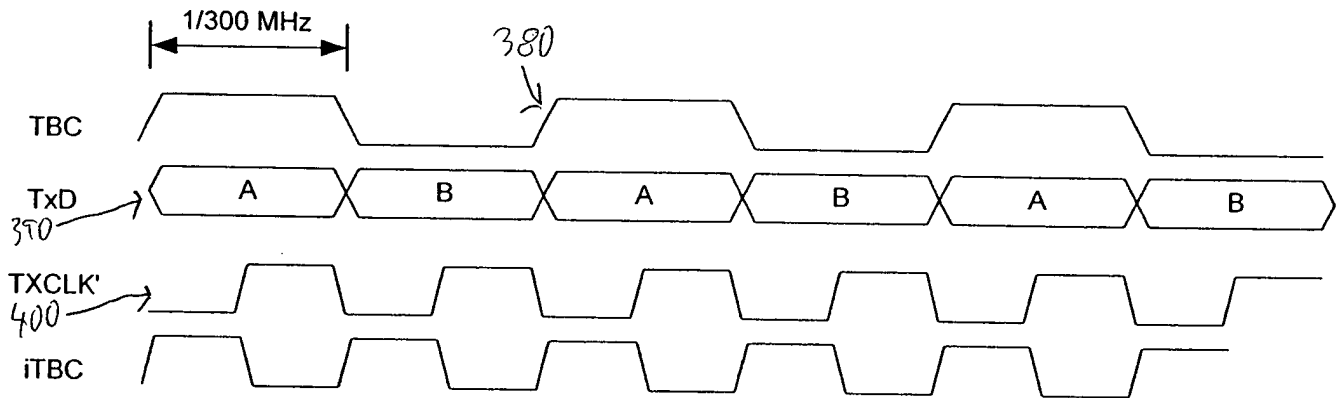


FIGURE 5C

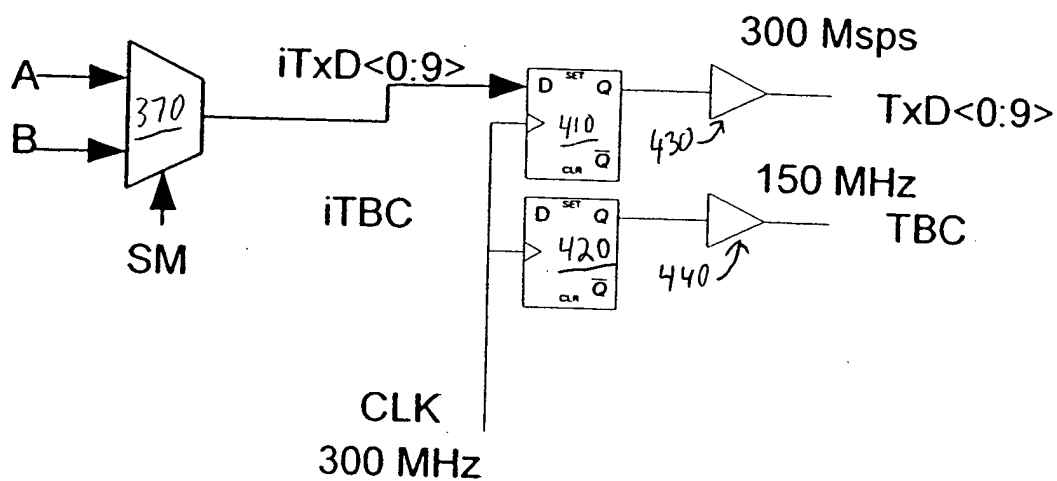


FIGURE 6

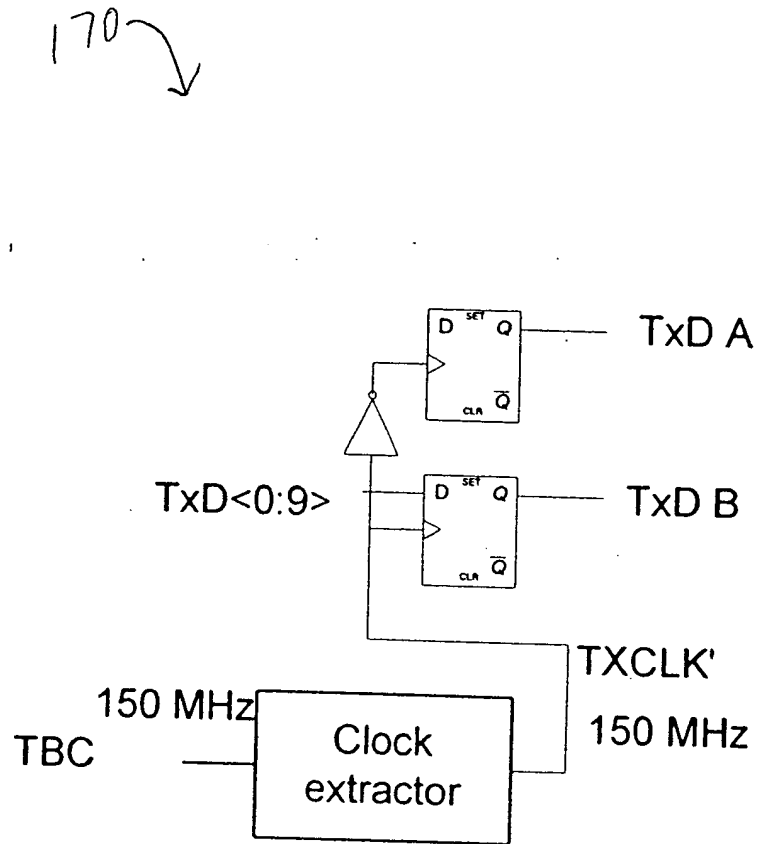


FIGURE 7



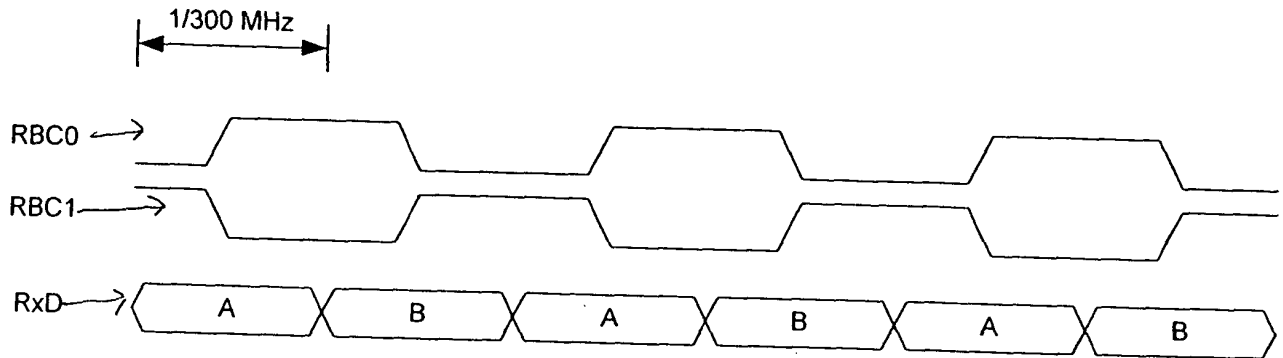


FIGURE 8

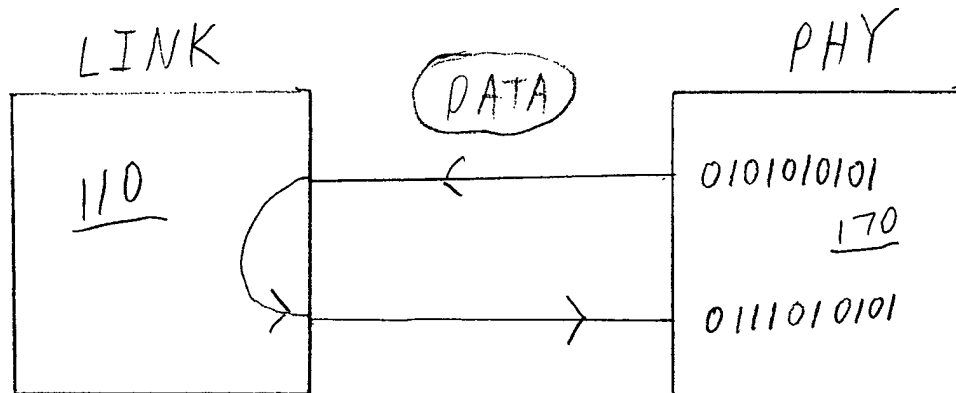


FIGURE 9A

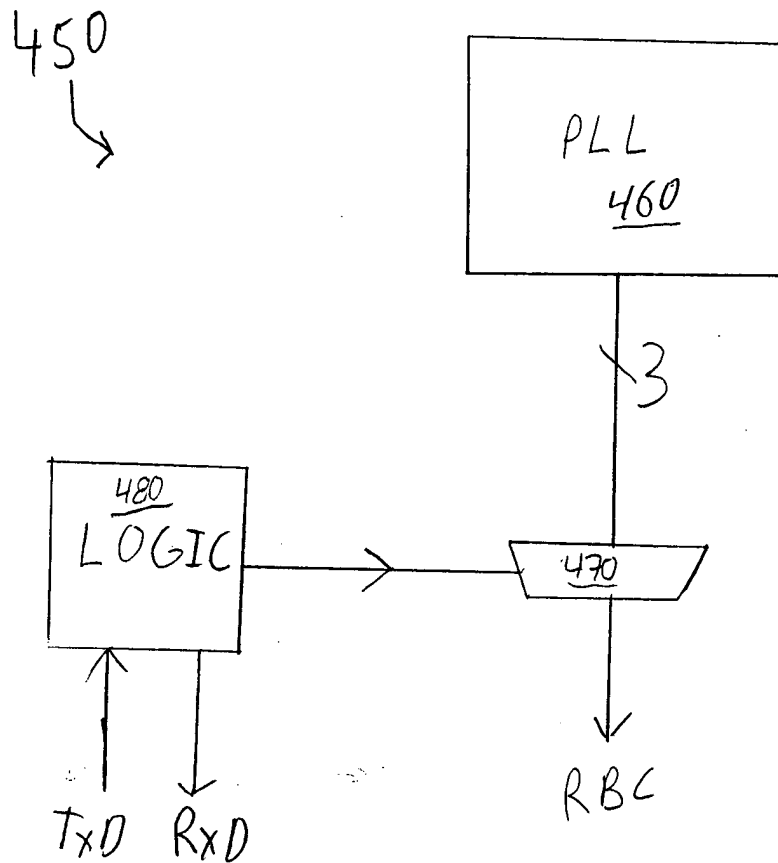


FIGURE 9B

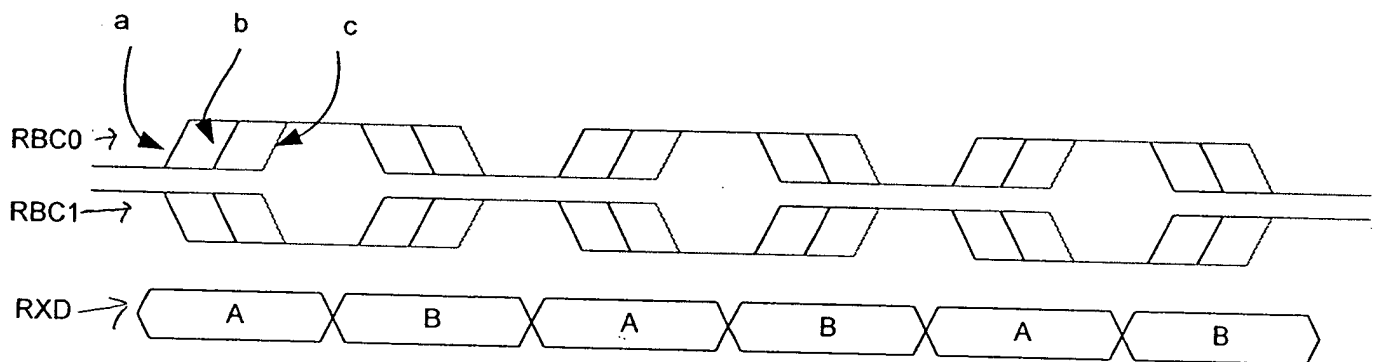


FIGURE 9C

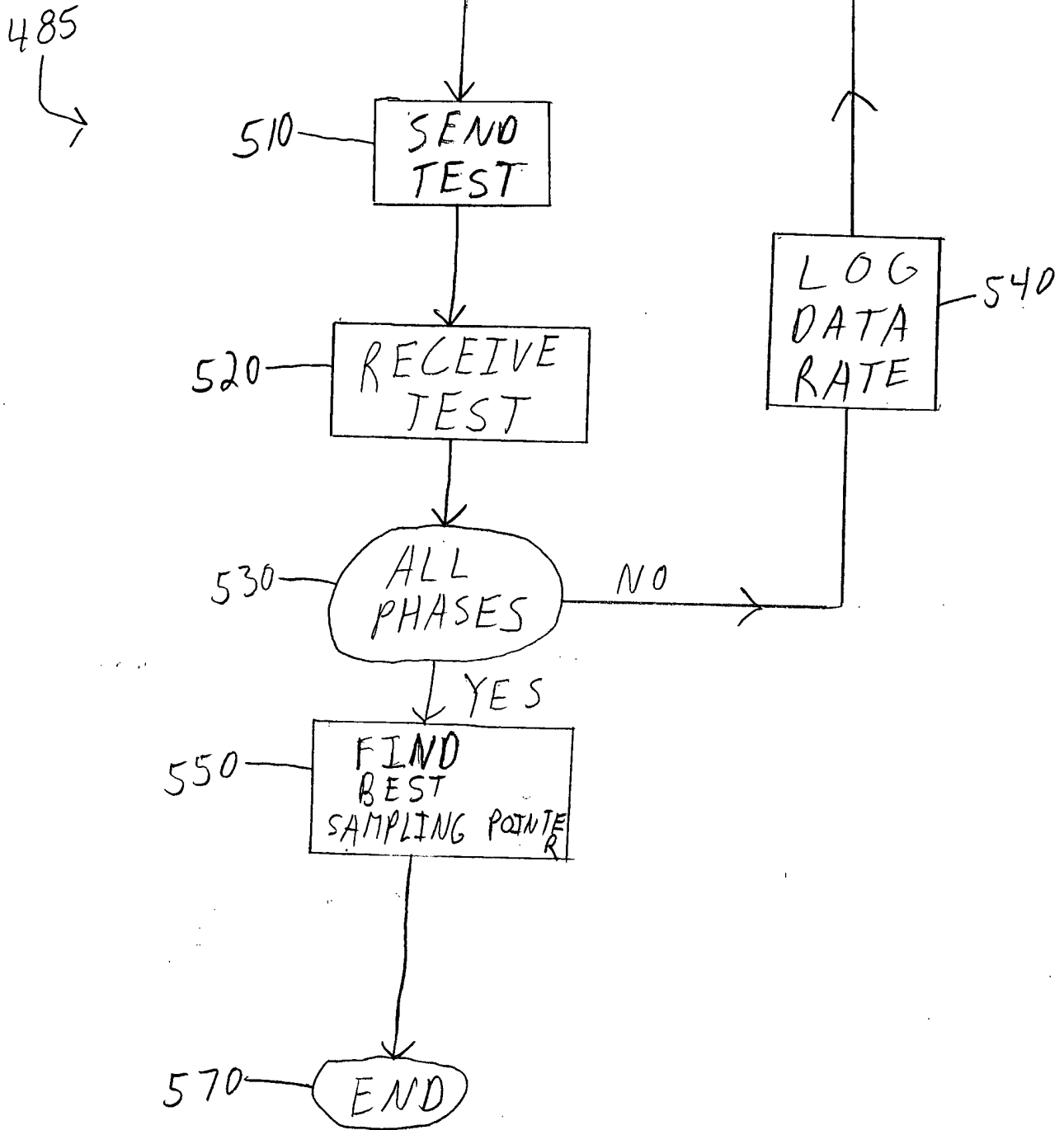


FIGURE 10

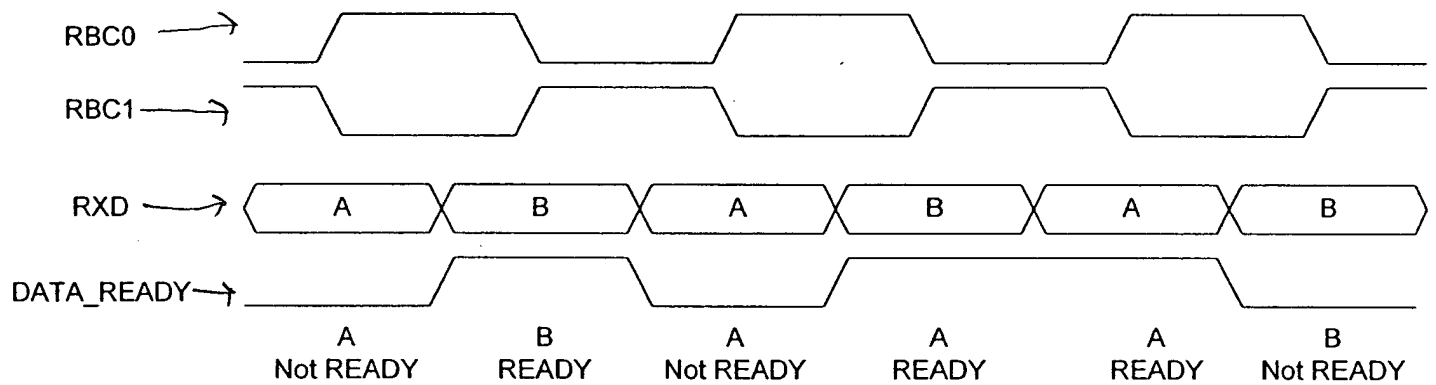


FIGURE 11

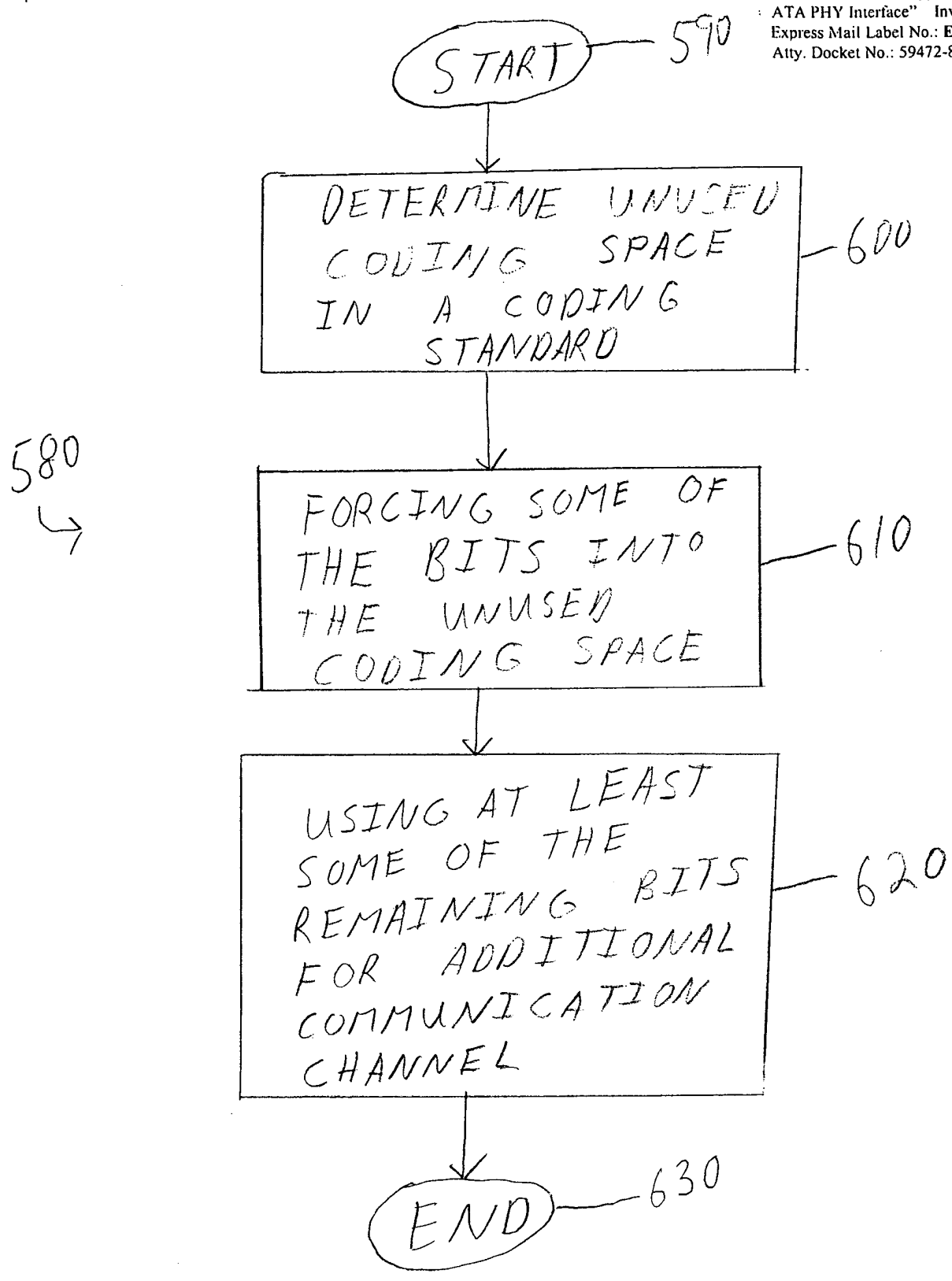


FIGURE 12

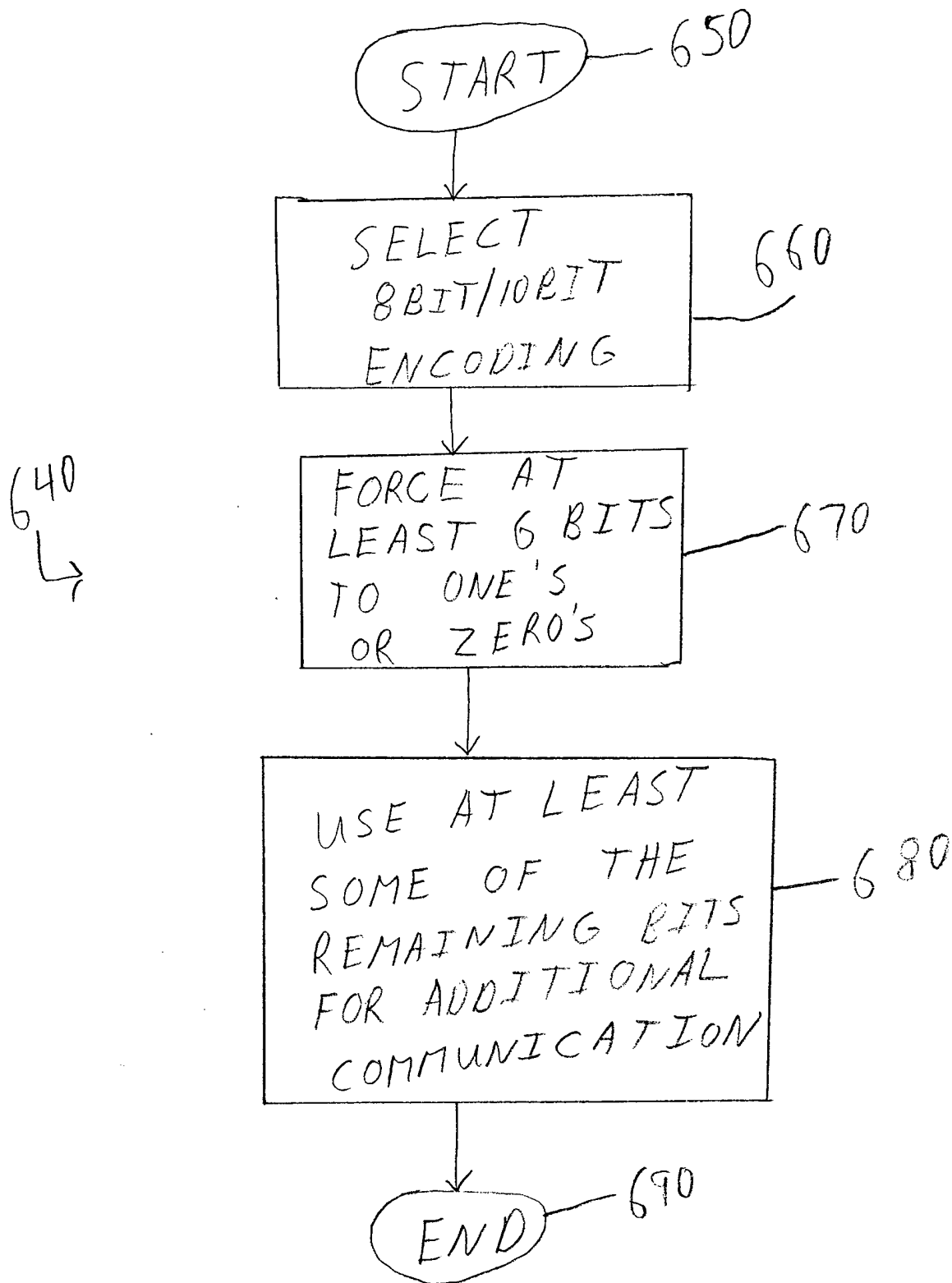


FIGURE 13A



700 → 1 1 1 1 1 1 ABCD  
                    0  
                    0  
                    0  
                    0  
710 → 0 0 0 0 0 0 ABCD

FIGURE 13B

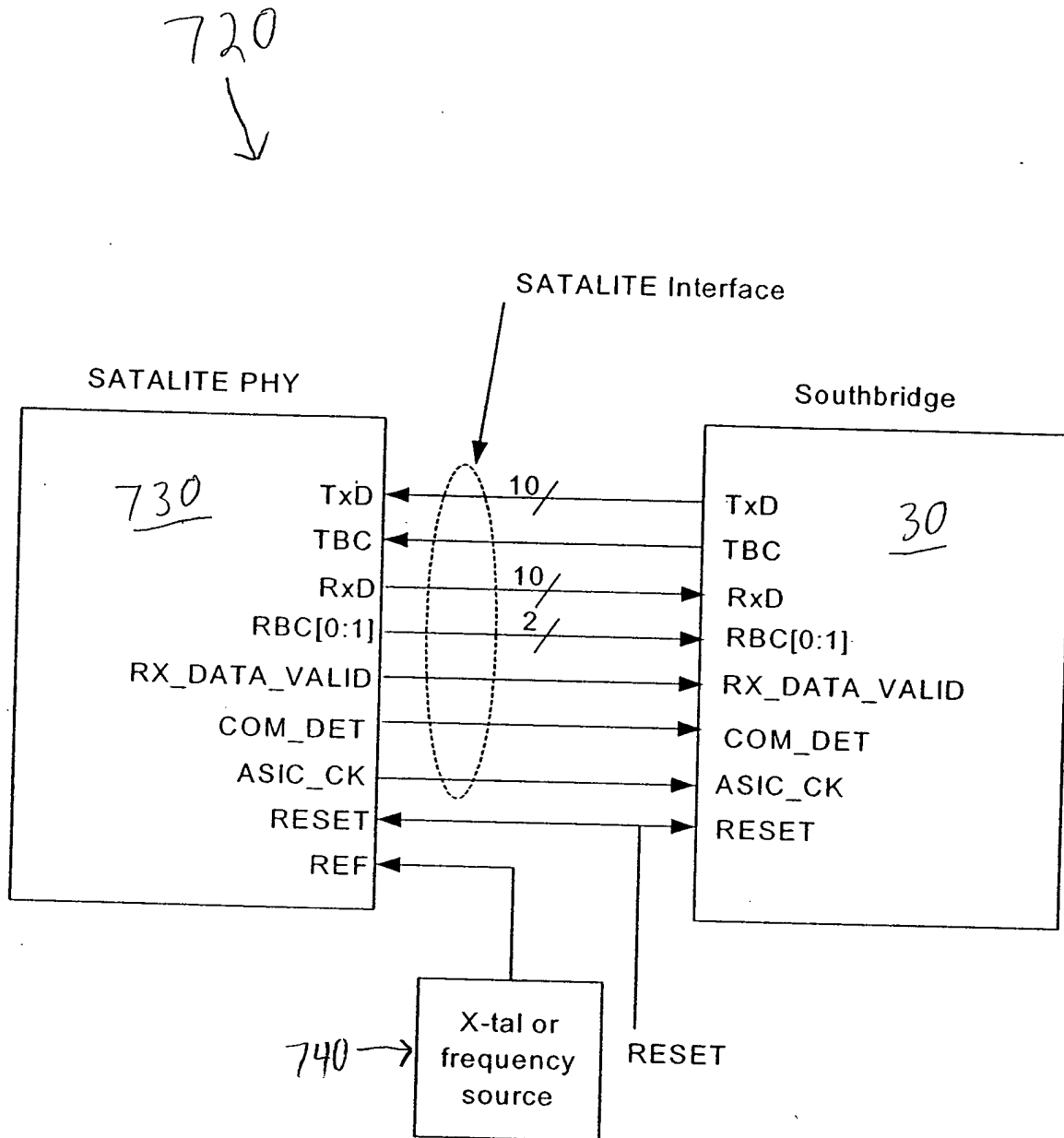


FIGURE 14



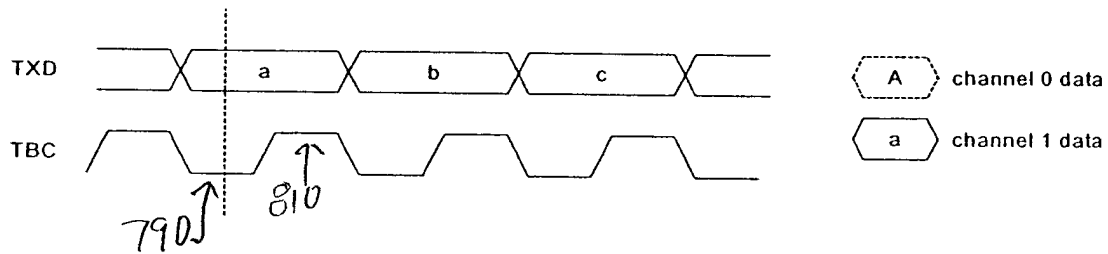
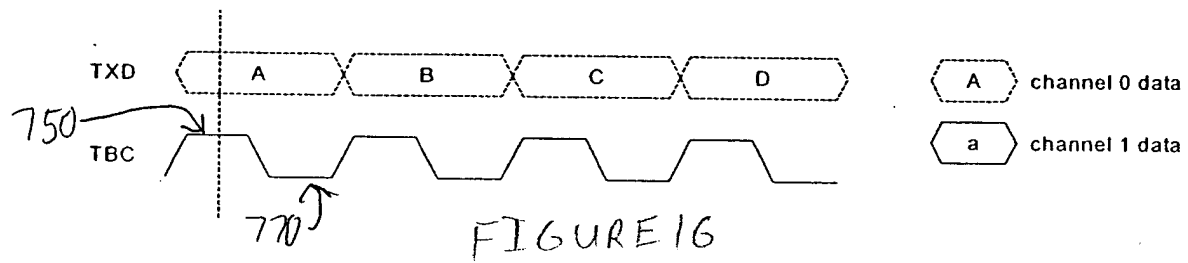


FIGURE  
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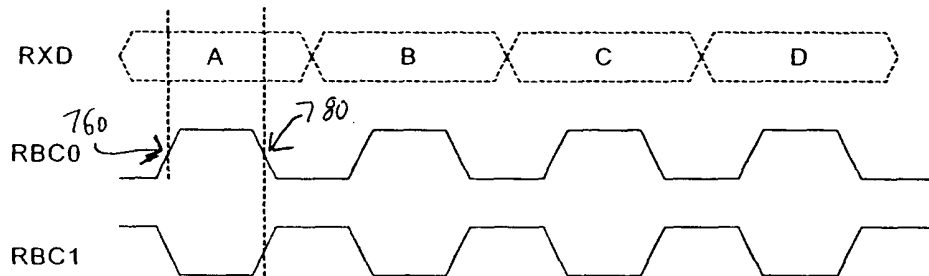
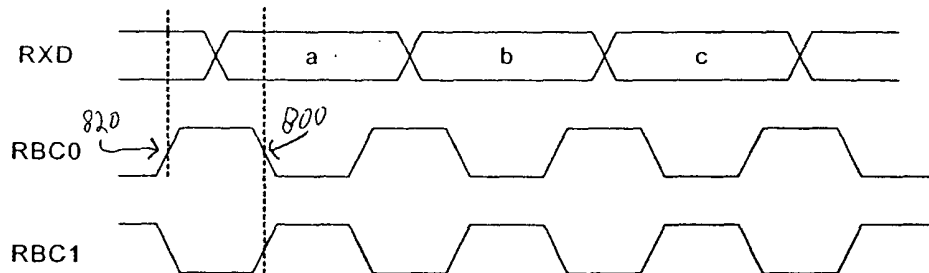


FIGURE  
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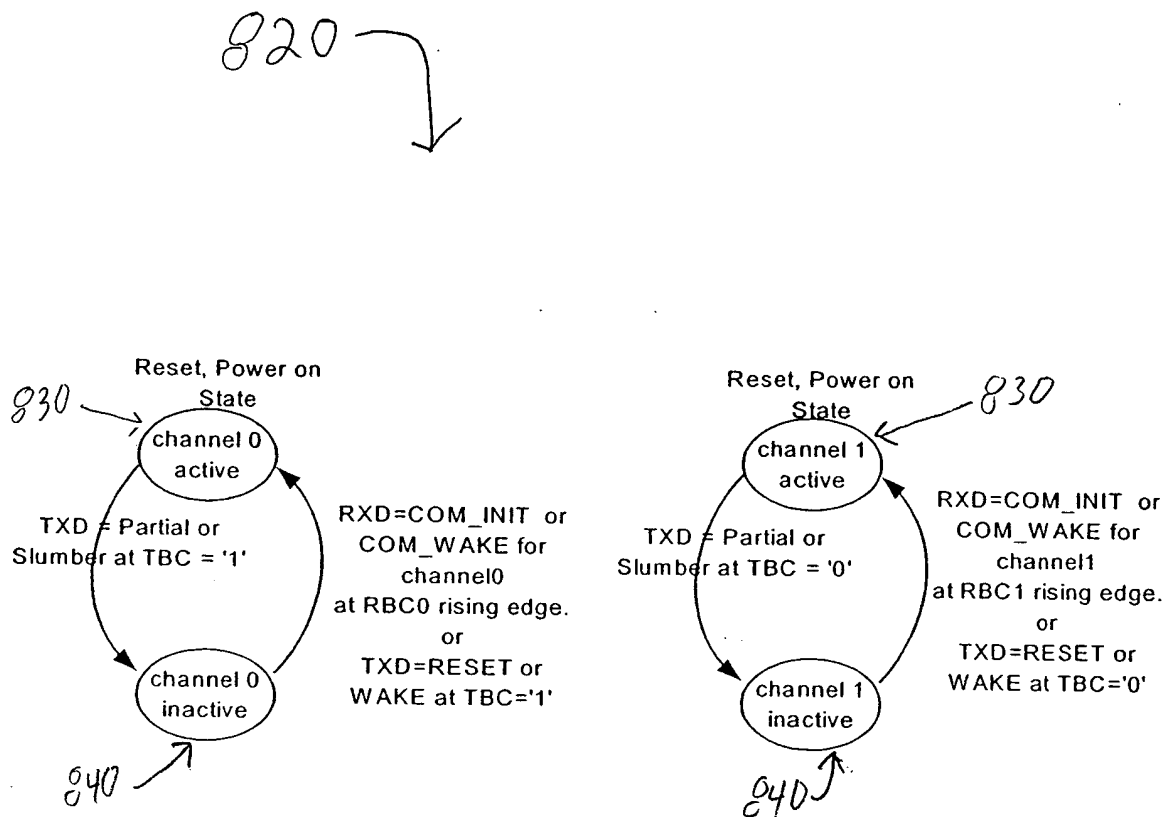


FIGURE 20

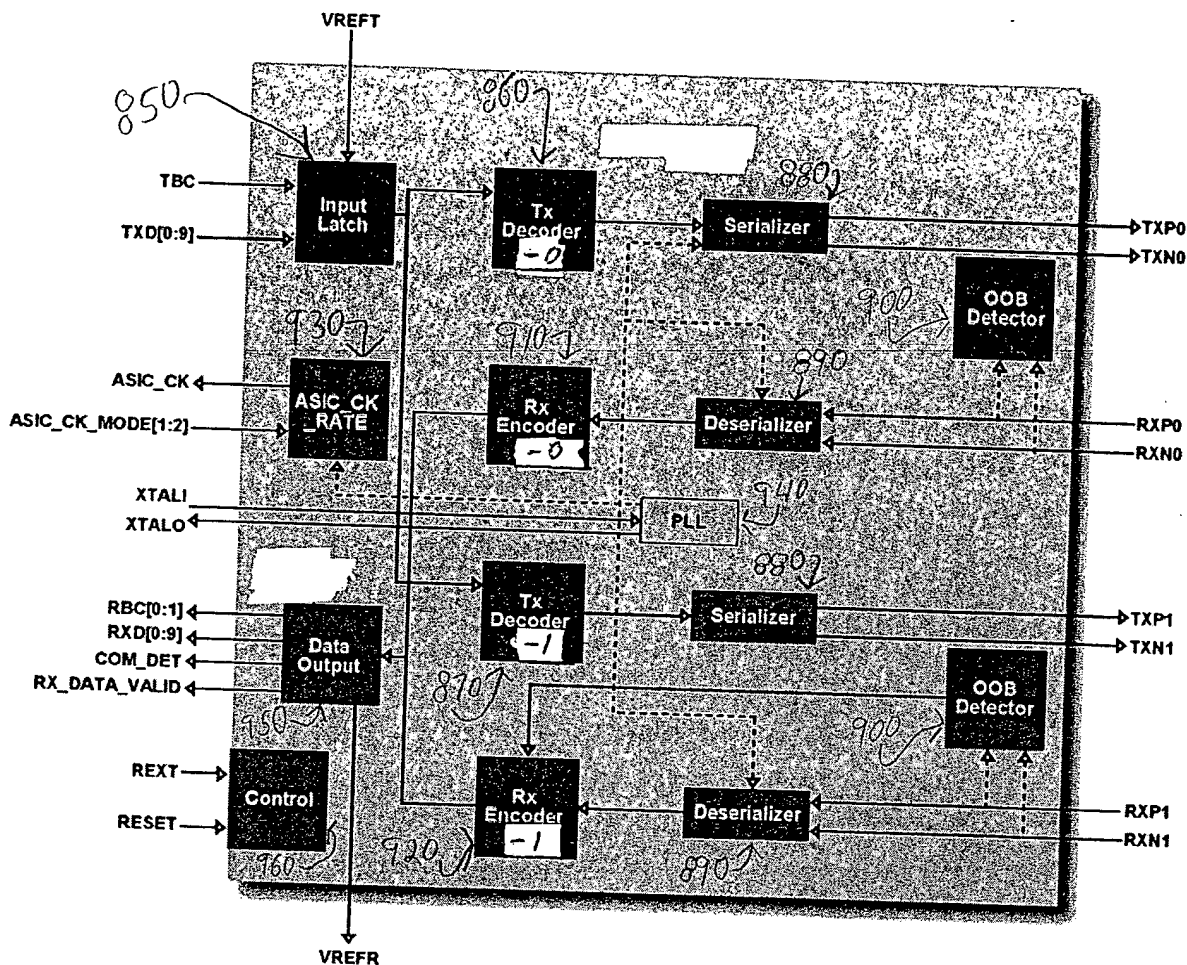


FIGURE 21

# RX encoder with two channel interface

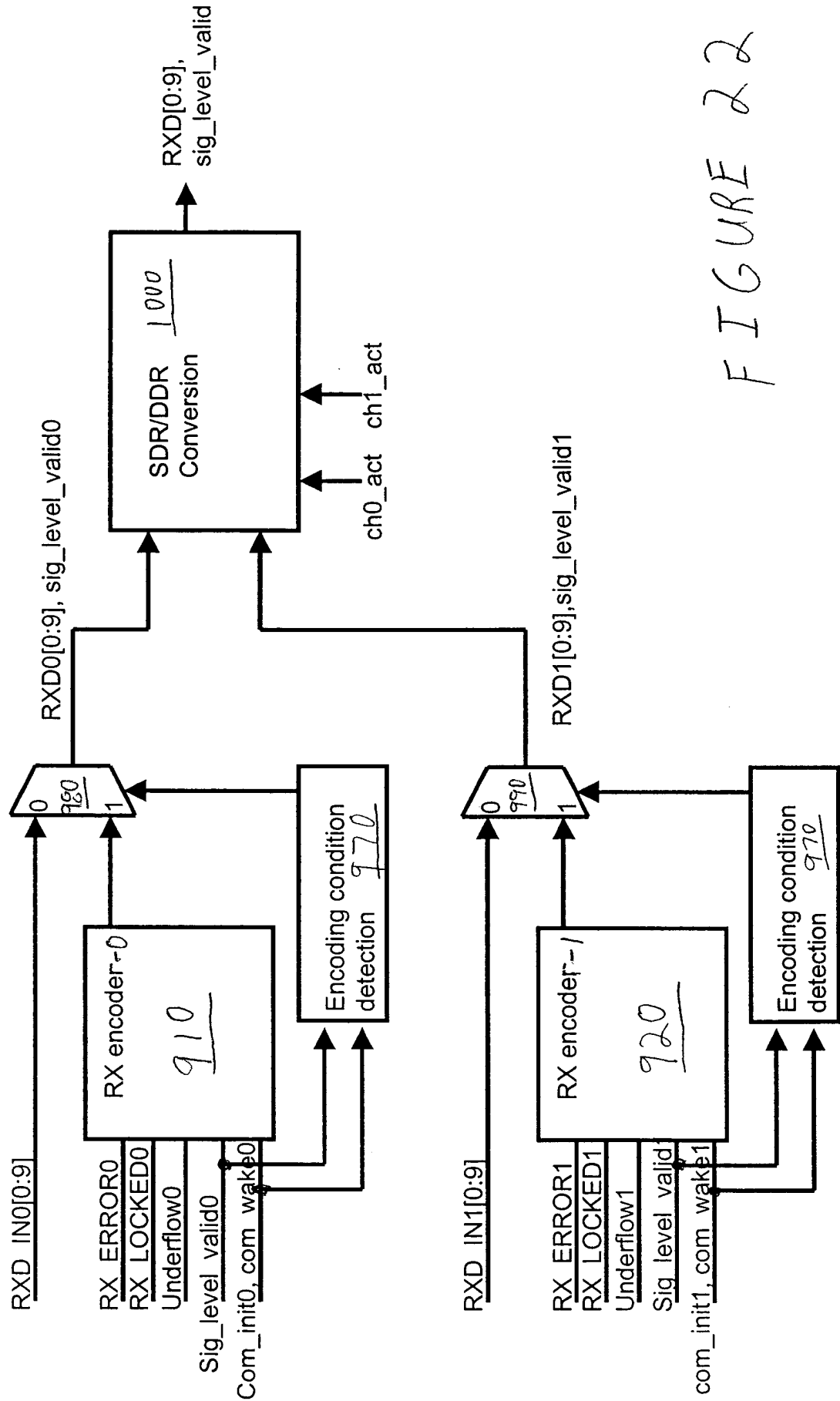


FIGURE 22



TX decoder with two channel interface

